36. (New) The method of claim 32, wherein the high resistivity semiconductor material has a resistivity between 10 ohm-m to 200 ohm-m.

REMARKS

Claims 1-8, 13-26, 31-32 and 34-36 remain in the present application, of which claims 1, 13, 22, 31 and 32 are independent. Claims 9-12, 27-30 and 33 have been canceled. Claims 13 and 31 have been rewritten in independent form to be placed in a condition for allowance. Claims 1, 21-22 and 32 have been amended, and new claims 34-36 have been added. Applicants respectfully request reconsideration and allowance of claims 1-8, 14-26 and 32, and that the allowability of claims 13 and 31 be maintained. Further, applicants respectfully request consideration on the merits and allowance of claims 34-36.

The Examiner has objected to the drawings under 37 CFR § 1.83(a) as not showing readout electronics, guard rings, field plates, light guides and scintillators, respectively. Applicants have proposed corrected drawings FIG. 1 and FIG. 2 that show readout electronics 25 and 125, respectively. Further, applicants have canceled claims 12 and 30 herein, and therefore, applicants respectfully submit that there is no need to show either guard rings or field plates on the drawings.

In addition, applicants have added new FIG. 6, which illustrates a scintillator 640 directly coupled to the entrance window 620 of a light sensitive array 610. Further, applicants have added new FIG. 7, which illustrates a scintillator 740 that interfaces with the entrance window 720 of a light sensitive array 710 via an interface 742 that serves as a light guide. No new matter has been added to any of these drawings. For example, claim 15 as filed recites "[t]he detector array . . . wherein the entrance window is directly coupled with the CsI(Tl) scintillator," and claim 16 as filed recites "[t]he

detector array . . . wherein the entrance window is coupled with the CsI(Tl) scintillator via an interface that functions as a light guide between the entrance window and the CsI(Tl) scintillator." In addition, the light sensitive arrays 610 and 710 have substantially the same structure as the light sensitive arrays 10 and 110 of FIGs. 1 and 2. Therefore, applicants respectfully request that these drawing changes be entered and the objections to the drawings be withdrawn.

Applicants have also deleted FIG. 3 (and reference to it in the specification), which is directed to an embodiment that is not suitable for the purposes of the present invention, and hence is not being claimed herein.

The Examiner has objected to the disclosure because of informalities, such as, a combination of prefix symbol, unit name, and unit symbol of length expressed as a sub-multiple. Applicants have amended the specification throughout to remove all informalities related to unit symbols. Therefore, applicants respectfully request that the objection to the disclosure be withdrawn.

The Examiner has objected to the specification as allegedly failing to provide proper antecedent basis for the claimed subject matter. In particular, the Examiner states that "the other scintillators recited in claims 17-19 and 21 are not found in the specification. Applicants have added new proposed FIGs. 6 and 7, and added corresponding paragraphs on page 16. No new matter has been entered since these scintillators are disclosed in the claims as filed (for example, claims 17-19 and 21). Therefore, applicants respectfully request that the objection to the specification be withdrawn.

The Examiner has rejected claims 20 and 21 under 35 U.S.C. § 112, first paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly

connected, to make and/or use the invention. According to the Examiner, the specification allegedly does not describe what it might mean for the entrance window to be "optimized" for receiving light from a scintillator. Additionally according to the Examiner, in view of the plurality of characteristics that the entrance window and any particular scintillator material might have, one skilled in the art does not have the necessary guidance as to how to make and/or use the invention.

Further, the Examiner has rejected claims 20 and 21 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. In particular, the Examiner states that one skilled in the art would be unable to decide whether a specific entrance window is "optimized" or not, especially as any particular scintillator is not a part of the scope of the claim. Applicants respectfully traverse as follows.

Those skilled in the art would understand that the term "optimized" refers specifically to: 1) maximizing quantum efficiency of the entrance window by maximizing its ability to transmit light at the wavelength of scintillation emission of the applied scintillator or light source; 2) minimizing reflections of light at the scintillator to photodetector or combination of scintillator to light guide and light guide to photodetector interfaces through the use of optical couplant materials and anti-reflective coatings; and 3) minimizing the resistivity of the entrance window contact in order to decrease noise due to series resistance. In view of this, applicants respectfully request that the rejection of claims 20 and 21 under 35 U.S.C. § 112, first and second paragraphs, be withdrawn.

The Examiner has also rejected claims 13, 31 and 33 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Since applicants

have canceled claim 33 herein, the rejection of claim 33 is now moot. Applicants have amended claims 13 and 31 to provide an antecedent basis to the term "the grid" in addition to rewriting them in independent form. Therefore, applicants respectfully submit that the rejection of claims 13 and 31 be withdrawn.

The Examiner has rejected claims 1, 2, 4, 5, 8-12, 22, 23, 25, 28-30, 26, 27 and 33 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,757,057 ("Dabrowski"). In addition, the Examiner has rejected claims 6 and 7 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Dabrowski. Further, the Examiner has rejected claims 3, 14-21, 24 and 32 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Dabrowski in view of U.S. Patent No. 5,773,829 ("Iwanczyk"). Since claims 9-12, 27-30 and 33 have been canceled herein, the rejection of claims 9-12, 27-30 and 33 is now moot.

The essential difference between the device disclosed by Dabrowski and the detector array in exemplary embodiments in accordance with aspects of the present invention is that Dabrowski describes a structure exclusively for an Large Area Avalanche Photodiode Device (LAAPD) and the detector array in the exemplary embodiments is for application to non-avalanching diodes. The differences between these classes of devices are significant as described below.

An LAAPD (e.g., as described by Dabrowski) must be realized using low resistivity silicon in the 30 ohm-cm to 100 ohm-cm (.3 ohm-m to 1 ohm-m) region (Dabrowski, Col. 5, lines 56-59) in order to achieve high enough electric field to facilitate the avalanche breakdown condition. The detector array in exemplary embodiments of the present invention is not an LAAPD and is realized using extremely high resistivity silicon in the 1,000 ohm-cm to 20,000 ohm-cm (10 ohm-m to 200 ohm-m) region (e.g., specification as filed, page 10, line 17-18) and this high resistivity is suitable for using much lower electric

fields so as to avoid breakdown. Thus, Dabrowski teaches away from the present invention.

To operate an avalanche diode, one must bring the device to extremely high bias voltages of between 2,000 and 3,000 volts (e.g., Dabrowski, Col. 1, line 50). At such high voltages it is typically not possible to fully deplete the structure from the p-n junction at the first surface of the LAAPD without catastrophic breakdown due to "short circuiting" of the LAAPD (Dabrowski, Col. 2, lines 45-53) in the absence of essential structures disclosed in Dabrowski, such as the cavity and/or grooves, beveled edges, and the like. The detector array of the present invention is biased at between -10 V to - 200 V typically (e.g., specification as filed, page 11, line 20-22) and may achieve full depletion or even over-depletion without any catastrophic breakdown since the electric field strength in the present invention is much lower than that required in Dabrowski. As such, the structures such as the cavity and/or grooves, beveled edges, and the like that are essential for the device of Dabrowski are not needed in the device of the present invention.

For example, for an LAAPD of Dabrowski to work, it is necessary that it includes a "cavity" (e.g., Dabrowski, 110 of Fig 1A, 210 of Fig 2A, 310 of Fig 3A, 510 of Fig 5A), and/or "grooves" (e.g., 660 Fig 6A). These features of the LAAPD (as is true also for the LAAPD beveled edges) are not methods of making the claimed product, but are instead critical elements of the device disclosed in Dabrowski. In fact, these are features without which it is not possible to realize an LAAPD as disclosed by Dabrowski. Once again, all disclosures in Dabrowski are specifically for solving problems associated with LAAPD fabricated using a low resistivity silicon, and neither anticipates nor suggests application to non-avalanche diodes fabricated on high resistivity silicon.

Further, Dabrowski discloses on Col. 4, line 31-33, "[a]dvantageously, with the grooves, the cavity does not have to be

formed as deeply into the silicon wafer or even formed at all." The literal meaning of this is that grooves must be provided unless there is a cavity in which case perhaps grooves may not be needed. In other words, one and/or the other must be provided for the LAAPD to work. Thus, the isolation grooves are a necessary part of the device structure and are there to avoid the catastrophic breakdown (or short circuiting) associated with the LAAPD as discussed above. It would not be readily apparent to one skilled in the art that in the absence of these requirements to avoid problems with avalanche breakdown, similar features could yield improvements in high resistivity non-avalanching diodes. The fact that each claim of Dabrowski is limited to LAAPD further evidences that Dabrowski did not envision anything beyond LAAPDs fabricated on low resistivity silicon.

Claim 1 recites in a relevant portion, "[a] detector array formed on a high resistivity semiconductor material having a first side and a second side . . . wherein the entrance window forms a junction with the high resistivity semiconductor material, and the detectors comprise pixelated ohmic contacts." Since such use of high resistivity semiconductor material to form a junction-side illuminated detector array is not disclosed by Dabrowki, claim 1 is not anticipated by Dabrowski. Therefore, applicants respectfully request that the rejection of claim 1 be withdrawn and that it be allowed.

Since claims 2-8, 14-21 and 34 depend, directly or indirectly, from claim 1, they incorporate all the terms and limitations of claim 1 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants respectfully request that the rejection of claims 2-8, 14-21 and 34 be withdrawn and that they be allowed.

Claim 22 recites in a relevant portion, "[a] method of forming a detector array on a high resistivity semiconductor material having a first side and a second side . . . wherein the entrance window forms a junction with the high resistivity semiconductor material, and the

detectors comprise pixelated ohmic contacts." Since such use of high resistivity semiconductor material to form a junction-side illuminated detector array is not disclosed by Dabrowki, claim 22 is not anticipated by Dabrowski. Therefore, applicants respectfully request that the rejection of claim 22 be withdrawn and that it be allowed.

Since claims 23-26 and 35 depend, directly or indirectly, from claim 22, they incorporate all the terms and limitations of claim 22 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants respectfully request that the rejection of claims 23-26 and 35 be withdrawn and that they be allowed.

Claim 32 recites in a relevant portion, "[a] composite detector array comprising a plurality of detector arrays, wherein at least one of the detector arrays includes a detector array formed on a high resistivity semiconductor material having a first side and a second side. . . wherein the entrance window forms a junction with the high resistivity semiconductor material, and the detectors comprise pixelated ohmic contacts." Since such use of high resistivity semiconductor material to form a junction-side illuminated detector array is not disclosed by Dabrowki, claim 32 is not anticipated by Dabrowski. Therefore, applicants respectfully request that the rejection of claim 32 be withdrawn and that it be allowed.

Since claim 36 depends from claim 32, it incorporates all the terms and limitations of claim 32 in addition to other limitations, which together further patentably distinguish it from the cited references. Therefore, applicants respectfully request that the rejection of claim 36 be withdrawn and that it be allowed.

In view of the foregoing amendments and remarks, applicants respectfully request allowance of claims 1-8, 14-26, 32 and 34-36 in addition to the allowable claims 13 and 31, and an early issuance of a patent. If there are any remaining issues that can be addressed over the telephone, the Examiner is invited to call applicants'

attorney at the number listed below.

Attached hereto is a marked-up version of the changes made to the above-identified application by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By 

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626/795-9900

JEJ/sd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On page 2, lines 8-19, please replace with the following paragraphs:

Other broad applications including radiation hardened detector arrays for high-energy physics research [~~, and new designs of avalanche imaging arrays (photodetectors with an internal gain)~~] would also benefit from a development of low cost, high-yield detector array structures.

Typical silicon photodiode arrays with parallel signal readout are based on (p+)-(n)-(n+) structures constructed on high resistivity [~~(0.1 - 10 k ohm-cm)~~] (1 - 100 ohm-m) silicon wafers. P+ contacts forming junctions in the n-type substrate are constructed in the form of a diode array. A common n+ contact forms an ohmic contact, and is used as an entrance window (light sensitive window).

On page 2, line 31 through page 3, line 9, please replace with the following paragraph:

In the back-side illuminated photodiodes, the (p+)-(n) junction array, which is created on the non-light sensitive side of the chip, is generally used only for signal readout and therefore can usually be bonded directly to the readout chip or circuitry without obstructing the light from a scintillator. The opposite side (ohmic side) is typically coupled to the scintillator for light detection. This type of array typically operates only in fully depleted mode, which usually requires reverse bias of more than 70 V for the standard [~~5000 ohm-cm~~] 50 ohm-m resistivity silicon or higher biases for lower resistivity material.

On page 5, line 25 through page 6, line 18, please replace with the following paragraphs:

The above and other features of the present invention may be more fully understood from the following detailed description, taken together with the accompanying drawings, wherein similar reference characters refer to similar elements throughout and in which:

FIG. 1 is a cross-sectional view of a detector array produced from high resistivity n-type Si (top) and back-side view (bottom) in an embodiment according to the present invention;

FIG. 2 is a cross-sectional view of a detector array produced from high resistivity p-type Si (top) and back-side view (bottom) in an embodiment according to the present invention;

~~[FIG. 3 is a cross-sectional view of an avalanche detector constructed from high resistivity n-type Si in an embodiment according to the present invention;]~~

FIG. ~~[4]~~ 3 is a top view of the topology of a detector array showing separate grids for changing of the pixel sizes by biasing appropriate grids in an embodiment according to the present invention;

FIG. ~~[5]~~ 4 is a top view illustrating the method for joint biasing of individual grid arrangements by coupling grids together; ~~[and]~~

FIG. ~~[6]~~ 5 is a top view illustrating the method for individually biasing the grid arrangements;

FIG. 6 is a cross-sectional view of a detector array coupled directly to scintillators and coupled with readout electronics in an exemplary embodiment according to the present invention; and

FIG. 7 is a cross-sectional view of a detector array coupled to scintillators via a interface that functions as a light guide and coupled with readout electronics in another exemplary embodiment according to the present invention.

On page 7, lines 18-26, please replace with the following paragraph:

The photodetector array construction of the present invention may have significant advantages in the mass production process due to lower operating bias voltages, significantly simplified testing, use of thicker Si wafers (less breakage during processing), and possible very high production yields. Use of thicker wafers opens up additional possibilities of processing 6" (instead of 4") (approximately 15 cm (instead of approximately 10 cm)) or even larger diameter wafers leading to the possibility of further reduction in production costs.

On page 8, lines 21-30, please replace with the following paragraph:

The detector array of the present invention may also be used as a radiation hardened detector for high-energy physics research for detection of particles, x-ray, or gamma rays. The radiation hardness of this structure may be achieved through simplified construction (lack of the field plates and excessive guard rings) and relatively low operating bias voltages. The present invention may also find other broad applications ~~[including, but not limited to, applications as novel designs for avalanche imaging arrays (photodetectors with an internal gain)]~~.

On page 10, lines 13-23, please replace with the following paragraph:

Referring now to the drawings and in particular to FIG. 1, a light sensitive array 10 in an embodiment according to the present invention is constructed from n-type silicon (Si) 14. The n-type Si 14 preferably is high resistivity Si, such resistivity preferably being between [~~1000 ohm-cm to 20,000 ohm-cm~~] 10 ohm-m to 200 ohm-m. The light sensitive array 10 has a common p^+ light sensitive contact

20 on the front-side and ohmic contacts implemented as a n^+ pixelated array 24 on the back-side. The n^+ pixels on the back-side preferably are coupled to readout electronics 25 via pre-amplifiers (not shown).

On page 11, line 26 through page 12, line 12, please replace with the following paragraph:

The operational bias voltage, $-V_B$ 34 applied to the p^+ light sensitive contact 20 may be lower by up to a factor of four than the bias voltage necessary to operate standard back-side illuminated silicon structures fabricated from identical starting materials. During testing of the light sensitive array 10, it is not required to measure each of the (thousands of) individual pixels at a great expenditure of time and resources. Instead, a complete evaluation of the array may be achieved with only two measurements. The first measurement is of the leakage current of the fully biased p^+ light sensitive contact 20 (without biasing the p^+ grid 28). The second measurement is of the leakage current of the fully biased p^+ grid 28 (without biasing the p^+ light sensitive contact 20). Measured values of the leakage currents less than [~~10 nA/cm^2~~] 100 $\mu A/m^2$ for the p^+ light sensitive contact 20 and p^+ grid 28 may be an indication of the proper operation of the entire light sensitive array 10. Leakage currents as low as [~~100pA/cm^2~~] 1 $\mu A/m^2$ may be encountered during these measurements.

On page 13, line 19 through page 14, line 5, please replace with the following paragraph:

The operational bias voltage, $+V_B$ 134 applied to the n^+ light sensitive contact 120 may be lower by up to a factor of four than the bias voltage necessary to operate standard back-side illuminated silicon structures fabricated from identical starting materials. During testing of the light sensitive array 110, it is not required to measure each of the (thousands of) individual pixels at a great

expenditure of time and resources. Instead, a complete evaluation of the array may be achieved with only two measurements. The first measurement is of the leakage current of the fully biased n^+ light sensitive contact 120 (without biasing the n^+ grid 128). The second measurement is of the leakage current of the fully biased n^+ grid 128 (without biasing the n^+ light sensitive contact 120). Measured values of the leakage currents less than [~~10 nA/cm²~~] 100 $\mu A/m^2$ for the n^+ light sensitive contact 120 and n^+ grid 128 may be an indication of the proper operation of the entire light sensitive array 110. Leakage currents as low as [~~100pA/cm²~~] 1 $\mu A/m^2$ may be encountered during these measurements.

On page 14, line 6 through page 15, line 27, please delete the paragraphs as follows.

~~[FIG. 3 is a block diagram of a light sensitive array (detector array) 12 according to one embodiment of the present invention. The light sensitive array 12 is constructed from n-type Si 14. The n-type Si 14 preferably is high resistivity Si such resistivity preferably being between 1000 ohm-cm to 20,000 ohm-cm. The light sensitive array 12 has a common p^+ junction electrode 20 on the front side and ohmic contacts implemented as an n^+ pixelated array 24 on the back side.~~

~~The light sensitive array 12 is similar to the light sensitive array 10 of FIG. 1 in that the light sensitive array 12 preferably is biased at the p^+ junction electrode 20 and the p^+ grid 28. In other embodiments, the p^+ grid 28 may not be biased. Instead, the front depletion region 32 may extend down to the p^+ grid 28.~~

~~The p^+ junction contact 20, which preferably covers the entire light sensitive array 12, preferably is biased at a sufficiently high voltage $-V_{AV}$ 38 to achieve a controlled avalanche effect (amplification through electron impact ionization). The p^+ junction contact 20 may also be referred to as an entrance window contact or as an entrance window.~~

~~To isolate the individual n^+ pixels 24, the inter pixel gap contains p^+ separation implants 26 that surround each pixel in the form of p^+ rings and/or a p^+ grid 28 created on the entire array. In the case of avalanche detector arrays, the electric field at the periphery 40 of the p+ junction contact 20 should be shaped in a particular manner so as to prevent premature surface breakdown.~~

~~This electric field shape may be achieved through an implementation of a beveled edge structure in the n-type Si 14. The bevel may be formed by removing n-type Si material from the edge of the light sensitive array 12 as represented by the broken lines 42, which form a right triangle with the cross-sectional edge of the n-type Si 14. The hypotenuses of the right triangles formed on the left and right sides of the n-type Si 14 indicate the slope of the bevel. The required shaping of the electric field at the periphery 40 may also be achieved through the use of guard rings and/or field plates.~~

~~In other embodiments, a p-type silicon may be used to implement a light sensitive array similar to the light sensitive array 12. In the light sensitive array implemented using the p-type silicon, the entrance window would be implemented with n^+ junction contact, the pixelated array would include p^+ pixels, and a grid on the back side would be implemented using n^+ implants.~~

~~The p+ grid implants 26 forming the grid pattern 28 in the present invention for a n-type substrate, and n+ grid implants 126 forming the grid pattern 128 in the present invention for a p-type substrate may be designed in a variety of ways including, but not limited to, possibility of separation of different sections of the grid with independent biasing or floating of their sections.]~~

On page 15, line 28 through page 16, line 21, please replace with the following paragraphs:

~~[Fig. 4]~~ FIG. 3 shows a construction of a grid pattern where high resistivity n-type Si 14 is used as the starting material. The

readout side of a device 50 in this case includes at least two grid patterns. One of the grid patterns 52 surrounds a second (interior) set of grid patterns 54. In this case, it is possible to achieve one pixel size by biasing the exterior sections of the grid 52 using voltage V_1, and to change the size of the pixels by biasing the interior sections of the grid 54 using voltage V_2. Using this method, the pixel size and the resulting spatial resolution of the detector array may be electronically regulated.

Referring now to [~~Figure 5~~] FIG. 4, the individual interior grid arrangements 54 may be jointly biased by a single externally applied voltage using V_2 if the individual grids are coupled via a conductive bridge 60 placed over an electrical insulation layer 62 which electrically isolates the interior grid 54 from the exterior grid 52. This may be implemented as a part of planar silicon device fabrication using standard photolithography tools, or after the wafers have been processed on individual detectors using physical masks to define areas for insulator and metal evaporations. Referring now to [~~Fig. 6~~] FIG. 5, the interior grids such as 54 and 56 may be individually biased through external connections to each such grid using voltages V_2 54, V_3 56, and the like.

In the Claims:

1. (Amended) A detector array formed on a high resistivity semiconductor material having a first side and a second side, the detector array comprising:

an entrance window formed on the first side, the entrance window being used to receive radiation; and

an array of detectors formed on the second side, one or more of the detectors being used for detecting the radiation received via the entrance window,

wherein the entrance window forms a junction with the high resistivity semiconductor material, and the detectors comprise pixelated ohmic contacts.

13. (Amended) [~~The detector array of claim 1,~~]

A detector array formed on a semiconductor material having a first side and a second side, the detector array comprising:

an entrance window formed on the first side, the entrance window being used to receive radiation;

an array of detectors formed on the second side, one or more of the detectors being used for detecting the radiation received via the entrance window; and

a grid surrounding one or more detectors,

wherein the entrance window forms a junction with the semiconductor material, and the detectors comprise pixelated ohmic contacts, and

wherein the grid surrounding the detectors comprises an inner grid surrounding one or more detectors and an outer grid surrounding the inner grid, wherein a first pixel size is achieved by biasing the inner grid and a second pixel size is achieved by biasing the outer grid, wherein the second pixel size is larger than the first pixel size.

21. (Amended) The detector array of claim 1, wherein the entrance window is optimized for receiving light from one selected from a group consisting of [~~light from~~] $CdWO_4$, NaI(Tl), LSO, BGO scintillators.

22. (Amended) A method of forming a detector array on a high resistivity semiconductor material having a first side and a second side, the method comprising the steps of:

forming an entrance window on the first side, the entrance window is for receiving radiation; and

forming an array of detectors on the second side, one or more of the detectors are used for detecting the radiation received via the entrance window,

wherein the entrance window forms a junction with the high resistivity semiconductor material, and the detectors comprise pixelated ohmic contacts.

31. (Amended) [~~The method of forming a detector array of claim 22,~~]

A method of forming a detector array on a semiconductor material having a first side and a second side, the method comprising the steps of:

forming an entrance window on the first side, the entrance window is for receiving radiation;

forming an array of detectors on the second side, one or more of the detectors are used for detecting the radiation received via the entrance window; and

forming a grid that surrounds one or more detectors,

wherein the entrance window forms a junction with the semiconductor material, and the detectors comprise pixelated ohmic contacts, and

wherein the grid surrounding the detectors comprises an inner grid surrounding one or more detectors and an outer grid surrounding the inner grid, wherein a first pixel size is achieved by biasing the inner grid and a second pixel size is achieved by biasing the outer grid, wherein the second pixel size is larger than the first pixel size.

32. (Amended) A composite detector array comprising a plurality of detector arrays, wherein at least one of the detector arrays

includes a detector array formed on a high resistivity semiconductor material having a first side and a second side, the detector array comprising:

an entrance window formed on the first side, the entrance window being used to receive radiation; and

an array of detectors formed on the second side, one or more of the detectors being used to detect the radiation received via the entrance window,

wherein the entrance window forms a junction with the high resistivity semiconductor material, and the detectors comprise pixelated ohmic contacts.